## CLAIMS

What is claimed is:

1. A computer system comprising a memory controller that includes a slot-based controller, wherein the slot-based controller is adaptable to launch a packet that straddles a first fixed packet slot and a second fixed packet slot.

2. The computer system of claim 1 wherein the packet launch position is advanced one half of a slot position relative second fixed packet slot.

3. The computer system of claim 1 wherein the packet is tagged with an attribute that indicates that the packet is straddling the first fixed packet slot and the second fixed packet slot.

4. The computer system of claim 3 wherein the attribute is a Rambus clock offset.

5. The computer system of claim 1 wherein the packet is a Rambus control packet.

6. The computer system of claim 1 wherein the memory controller further comprises a Rambus Asic Cell (RAC), wherein the RAC interfaces with a high frequency expansion channel.

7. The computer system of claim 6 wherein the slot-based controller comprises:

a scheduler;

a rules checker coupled to the scheduler;

a future packet queue coupled to the scheduler and the rules checker; and

a past packet queue coupled to the future packet queue, the scheduler and the rules checker.

8. The computer system of claim 6 wherein the rules checker uses entries in the past packet queue to validate future slot choices for the scheduler.

9. The computer system of claim 7 wherein the past packet queue and the future packet queue are unidirectional shift registers.

10. The computer system of claim 7 wherein the slot-based controller further comprises packet driving logic coupled to the RAC and the scheduler.

11. The computer system of claim 6 further comprising:

an expansion channel coupled to the RAC within the memory controller; and

a repeater coupled to the expansion channel.

12. The computer system of claim 11 further comprising:

a stick channel coupled to the repeater; and

a plurality of memory devices coupled to the stick channel.

13. The computer system of claim 12 wherein the memory devices are Rambus Dynamic Random Access Memories (RDRAMs).

14. The computer system of claim 11 further comprising a plurality of memory devices coupled to the expansion channel.

15. A memory controller comprising a slot-based controller adaptable to launch a packet that straddles a first fixed packet slot and a second fixed packet slot.

16. The memory controller of claim 15 wherein the packet launch position is advanced one half of a slot position relative second fixed packet slot.

17. The memory controller of claim 15 wherein the packet is tagged with an attribute that indicates that the packet is straddling the first fixed packet slot and the second fixed packet slot.

18. The memory controller of claim 17 wherein the attribute is a Rambus clock offset.

19. The memory controller of claim 15 wherein the packet is a Rambus control packet.

20. The memory controller of claim 15 wherein the memory controller further comprises a Rambus Asic Cell (RAC), wherein the RAC interfaces with a high frequency expansion channel.

21. The memory controller of claim 20 wherein the slot-based controller comprises:

a scheduler;

a rules checker coupled to the scheduler;

a future packet queue coupled to the scheduler and the rules checker; and

a past packet queue coupled to the future packet queue, the scheduler and the rules checker.

22. The memory controller of claim 21 wherein the rules checker uses entries in the past packet queue to validate future slot choices for the scheduler.

23. The memory controller of claim 21 wherein the past packet queue and the future packet queue are unidirectional shift registers.

24. The memory controller of claim 21 wherein the slot-based controller further comprises packet driving logic coupled to the RAC and the scheduler.

25. A slot-based controller comprising:

a scheduler;

a rules checker coupled to the scheduler;

a future packet queue coupled to the scheduler and the rules checker; and

a past packet queue coupled to the future packet queue, the scheduler and the rules checker;

wherein the slot-based controller is adaptable to launch a packet in advance of a predetermined packet slot.

26. The slot-based controller of claim 25 wherein the advance packet launch is accomplished by straddling the packet on a first fixed packet slot and a second fixed packet slot, wherein the first packet slot is designated for a previously scheduled packet.

27. The memory controller of claim 25 wherein the past packet queue and the future packet queue are unidirectional shift registers.

28. The memory controller of claim 25 wherein the slot-based controller further comprises packet driving logic coupled to the RAC and the scheduler.